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**FIELD EMITTER ARRAY RF AMPLIFIER DEVELOPMENT PROJECT
ARPA CONTRACT #MDA 972-91-C-0028
PHASE ONE, OPTION 1**

**QUARTERLY R&D STATUS/TECHNICAL REPORT #8
7/16/93 - 10/15/93**

**SPONSORED BY:
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ARPA / DSO**

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13. ABSTRACT (Maximum 200 words) The program goals of > 5 mA total anode current at current density of > 5 A/cm ² were achieved with a 1,197 tip array. Single tip devices from two separate wafers operated at > 1 μ A for over 24 hours. Successful electrical testing was performed on a 44,460 tip array. The in-house DC testing program has evaluated an average of 2.5 devices per workday since July 30, 1993. Out of 139 devices tested, 63 or 45% produced acceptable anode current at gate voltage below 250 V. Refinements continue at various steps in the process flow. More rigorous uniformity requirements have resulted in modification of the initial photolithography steps. Various gate metal systems are being tested to maximize device test performance. Development of low work function and metal coatings has focused on the optimization of the deposition process for tantalum nitride, and the development of processes for lanthanum hexaboride and zirconium carbide. The chemical composition, resistivity, and growth rate of the films is being analyzed. Theoretical calculations of the emission area and field enhancement factor for field emitter arrays were made using data collected from devices tested at MCNC. The resulting data compared favorably with <i>a priori</i> simulation results.				
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Title of Work: Field Emitter Array RF Amplifier Development Project
ARPA Contract #MDA 972-91-C-0028
Phase One, Option 1

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MCNC Field Emitter Array RF Amplifier Development Project
Phase One, Option 1: Cathode Technology Development
ARPA Contract MDA 972-91-C-0028

Eighth Quarter – October 1993

Key Ideas

Develop field emitter arrays with a cutoff frequency above 1 GHz, total current greater than 5 mA, and 5 A/cm² current density with the gate electrode potential less than 250V. Demonstrate these characteristics for greater than 1 hour lifetime.

Reduce capacitance and increase transconductance of field emitter arrays to improve frequency response. Focus on development of tall emitter columns to minimize capacitance. Evaluate low work function materials and metals as emitter surface coatings, reduce gate dimensions, and improve tip sharpening to increase transconductance. Fabricate large arrays with dense tip spacing to increase total current.

Examine various test methods to permit characterization of more devices per test cycle.

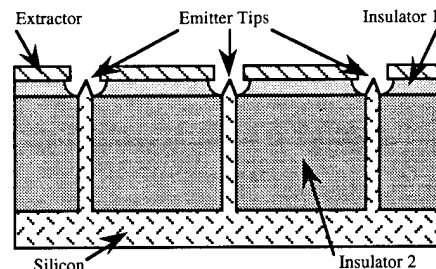
Major Accomplishments:

Second fabrication run of 2 μ m column devices with the new mask is complete. The remaining contract runs are proceeding on schedule, with consideration for equipment delays. Lot origination for the final two runs is complete and one is in processing.

Total current > 5 mA at current density > 5 A/cm² has been demonstrated. A single tip device delivered > 1 μ A at a gate potential of 200 V for 48 hours. DC test data shows yield on a 44,460 tip array. Measurement of the anode current was limited by the anode power supply. MCNC capital has been applied to purchase a larger supply. Equipment for whole-wafer testing has been received and is being installed.

Low work function and metal coating processes have been developed. Coated devices have been produced and are being tested.

MCNC Silicon Field Emitter with Column



Major Milestones – This and upcoming quarter:

Deliver sample devices for testing and SEM inspection data from second device fabrication run of 2 μ m column emitters. Characterize DC performance of devices from this run. Complete processing on device fabrication runs of 4 and 6 μ m column devices. Incorporate low work function and metal coatings into fabrication process flow.

Complete installation and setup of the whole-wafer test system. Continue the DC characterization and reliability testing program for Option 1 devices. Develop cooled anode for greater power density. Characterize and control the *in-situ* plasma cleaning system.

Refine the equipment used in the in-house RF testing program to improve the signal to noise ratio for measurements at high frequencies. Expand the frequency range of the in-house test system. Prepare 4 μ m devices for testing when completed. Evaluate results from RF testing at Litton subprogram site.

Field Emitter Array RF Amplifier Development Project Phase 1, Option 1

I. Executive Summary

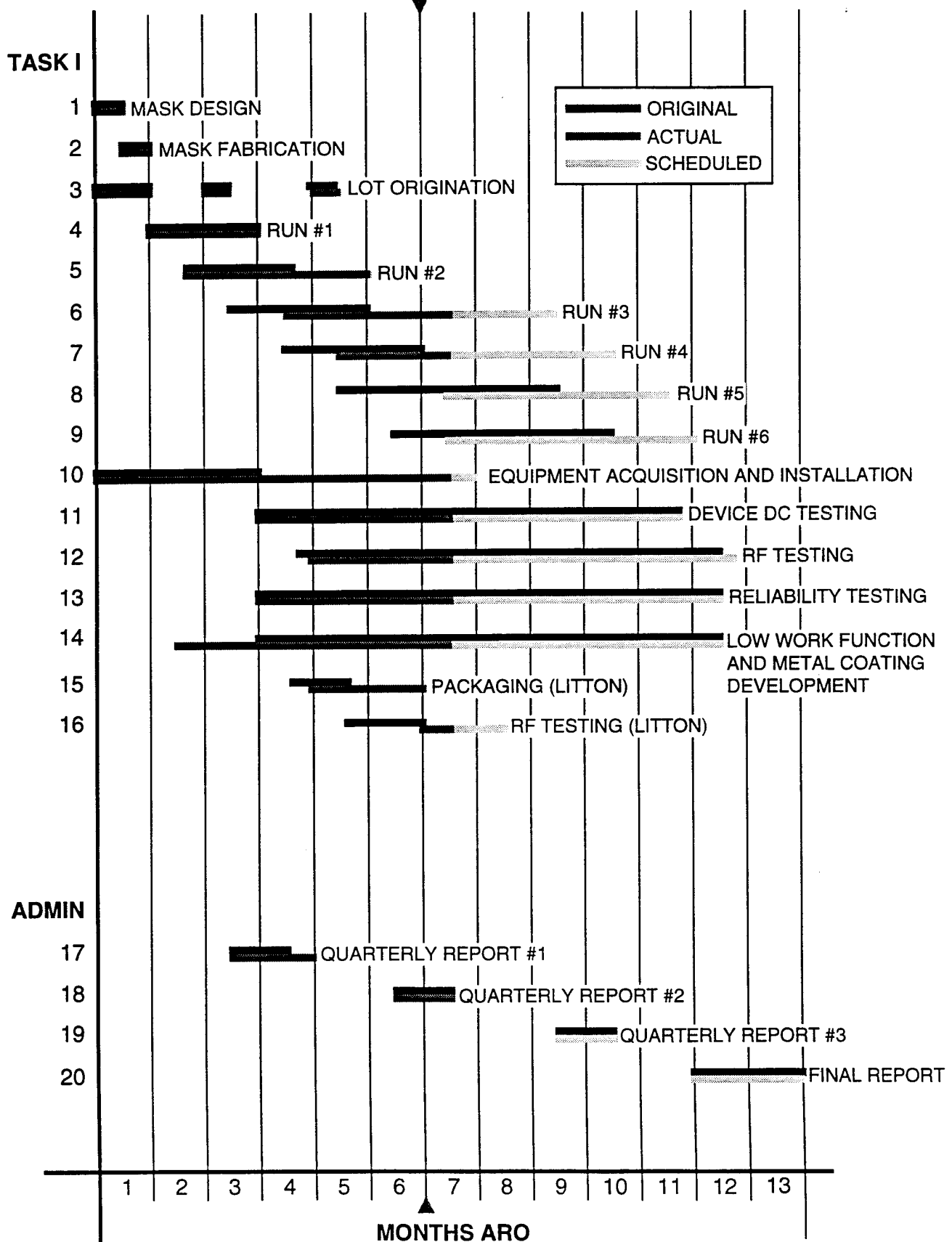
- Successful electrical testing was performed on 44,460 tip array. The program goals of > 5 mA total anode current at a current density of > 5 A/cm² were achieved with a 1,197 tip array. Gate voltage less than 200 V, emission efficiencies around 99%. New power supply and data acquisition equipment ordered with MCNC capital. Single tip devices from two separate wafers operated at > 1 μ A for over 24 hours.
- The in-house DC testing program has evaluated an average of 2.5 devices per workday since July 30, 1993. Out of 139 devices tested, 63 or 45% produced acceptable anode current at a gate voltage below 250 V.
- High-frequency testing is underway, both in-house and at Litton subprogram site. Test results are expected in the next quarter.
- The first two runs of 2 μ m column devices are finished. Arrays of 232,630 tips have been successfully fabricated and are being electrically tested. Two fabrication runs of 4 μ m column devices have been started and are proceeding on a revised schedule after delays in the initial photolithography step. The lot origination process for the 6 μ m column devices is complete.
- Refinements are continuing at various steps in the process flow. More rigorous uniformity requirements have resulted in modification of the initial photolithography steps. Different tip formation and sharpening methods are being evaluated. Various gate metal systems are being tested to maximize device test performance.
- An *in-situ* plasma cleaning system was installed and evaluated in the test chamber. Additional testing is needed to bring the cleaning process under control. The whole-wafer test system is partially complete, having been delayed by the installation of the plasma system. Final installation is expected to be complete in the next quarter.
- Development of low work function and metal coatings has focused on the optimization of the deposition process for tantalum nitride, and the development of deposition processes for lanthanum hexaboride and zirconium carbide. The chemical composition, resistivity, and growth rate of the deposited films is being analyzed by several methods.
- A device serialization method was implemented to improve record keeping on field emitter device testing.
- Theoretical calculations of the emission area and field enhancement factor for field emitter arrays were made using data collected from devices tested at MCNC. The resulting data compared favorably with *a priori* simulation results.

II. Milestone Status:

Task	Completion Date	
	Original	Complete Expected
Milestones		
Complete design and fabrication of new reticle set. Complete lot origination process for two runs of 2 μ m column emitter arrays. (MCNC)	5/93	5/93
Complete first run of field emitter arrays (2 μ m column). Complete lot origination process for two runs of 4 μ m column field emitter arrays. (MCNC)	7/93	8/93
Complete acquisition and installation of whole wafer DC test and RF measurement equipment. Begin in-house device DC characteristics and reliability testing program. (MCNC and Duke)	7/93	11/93
Begin low work function and metal coating development. (MCNC)	7/93	6/93
Complete second run of field emitter arrays (2 μ m column). Deliver devices to Litton subprogram for packaging and RF testing. (MCNC)	9/93	10/93
Begin in-house device RF testing program. (MCNC)	8/93	8/93
Complete third run of field emitter arrays (4 μ m column). Complete lot origination process for two runs of 4 or 6 μ m column field emitter arrays. (MCNC)	10/93	12/93
Complete packaging, begin RF testing of field emitter amplifier modules. (Litton)	9/93	10/93
Complete fourth run of field emitter arrays (4 μ m column). (MCNC)	10/93	1/94
Complete RF testing of field emitter amplifier modules. (Litton)	10/93	12/93
Complete fifth run of field emitter arrays (4 or 6 μ m column). (MCNC)	1/94	2/94
Complete sixth run of field emitter arrays (4 or 6 μ m column). (MCNC)	2/94	3/94
Complete all contract activities. Deliver devices, data, and other related material to ARPA. Complete and deliver final report according to contract stipulations. (MCNC)	4/94	4/94

Task	Completion Date	
	Original	Complete Expected
Deliverables		
Plots of new mask design set available for inspection by ARPA personnel if desired.	5/93	5/93
Sample devices from the first run of field emitter arrays (2 μ m column) with SEM inspection data.	7/93	8/93
First quarterly R&D status/technical report.	8/93	8/93
Sample devices from the second run of field emitter arrays (2 μ m column) with SEM inspection data. Performance data from first run.	8/93	11/93
Sample devices from the third run of field emitter arrays (4 μ m column) with SEM inspection data. Performance data from second run.	9/93	12/93
Sample devices from the fourth run of field emitter arrays (4 μ m column) with SEM inspection data. Performance data from third run.	10/93	1/94
RF amplifier module performance data from Litton subcontract.	10/93	12/93
Second quarterly R&D status/technical report.	11/93	11/93
Sample devices from the fifth run of field emitter arrays (4 or 6 μ m column) with SEM inspection data. Performance data from fourth run.	1/94	2/94
Sample devices from the sixth run of field emitter arrays (4 or 6 μ m column) with SEM inspection data. Performance data from fifth run.	2/94	3/94
Third quarterly R&D status/technical report.	2/94	2/94
Low work function and metal coating development results. Performance data from sixth run. Reliability test data for all devices. Final Technical Report – Option 1.	4/94	4/94

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III. Technical Progress:

1.0 Electrical testing and high-frequency performance measurements.

1.1 The largest working array so far is DOP1-1823-06-Q4, a 0.014 cm^2 array with 44,460 tips, tested September 23. With 120 V applied to the gate electrode, 6.991 mA of anode current was measured with only $8.65 \mu\text{A}$ of gate current. The measured data is shown in Figure 1. This represents a current density of 0.5 A/cm^2 with an emission efficiency of 99.8%. This current level may not be representative of maximum array performance, since the anode power supply is current limited to 7 mA.

The anode voltage for this test was 500 V, and the chamber pressure was around 2×10^{-8} Torr. That current level was only maintained for a short time, as the gate current and chamber pressure both began to rise dramatically. At this point, the gate voltage was lowered so that the array was emitting around 1 mA until the pressure in the chamber dropped back to its pre-test level. Another I-V curve was taken, that yielded maximum anode current of 3.680 mA with an applied gate voltage of 140 V and gate current around $40 \mu\text{A}$.

The anode supply limit was reached twice during testing on September 30. DOP1-2323-10-L3, a 0.0056 cm^2 array with 6,648 tips delivered anode current of 6.0 mA at 110 V with $2.58 \mu\text{A}$ of gate current. The measured data is shown in Figure 2. The array was tested again with the power supply current limiting defeated. The device delivered 8.9 mA of anode current at a gate voltage of 180 V with only $5 \mu\text{A}$ of gate current for a few moments before the gate electrode shorted to the substrate. In this test mode, the anode voltage is quite unstable, which likely contributed to the destruction of the device.

Also on September 30, DOP1-2323-10-A5, a 0.001 cm^2 array with 1,197 tips, ran at an average anode current of 5.486 mA, peaking to 6.930 mA on one occasion. The applied gate voltage was 150 V, and the average gate current was $2.26 \mu\text{A}$. Measured data for this device is shown in Figure 3. In this case, average current density was over 5 A/cm^2 with an average emission efficiency of 99.95%. This represents an average per-tip current of $4.58 \mu\text{A}$.

The high emission efficiency shown by these devices results from a combination of an increase in the measured anode current and a significant reduction in measured gate current. This reduction was observed with the introduction of a new anode used in the DC test system. Previously, the anode was constructed of various metals such as copper, brass, tungsten, or aluminum foil coated with titanium. These anodes exhibited adequate electrical performance in terms of capturing anode current, but the observed emission efficiencies were near 90%. A new anode was constructed from 20 mil thick crystalline graphite in a metal holder.

One motivation behind the use of graphite is the relatively low intensity of backscattered electrons produced by incidence of electron beams on elements with low atomic number. It is also a common anode material in high power microwave tubes. Additionally, the method of construction of this anode allows it to be placed much closer to the device under test. Thus far, however, there is no conclusive information that would indicate the reduction in gate current results solely from the use of the new anode.

An anode power supply capable of delivering higher current is being purchased with MCNC capital equipment funds to increase the range of measurement. Also, the series resistors in the anode and gate leads are being reduced in value to allow more current flow with lower voltage drops and power dissipation. These resistors are required both to protect the devices under test and the anode and gate power supplies. It would seem that their value would be an arbitrary choice for DC testing. However, with a 1 M Ω resistor in series, the effective anode voltage drops by 1000 V per mA of anode current. Additionally, the resistor will dissipate 1 W of power per mA, requiring the use of a larger power resistor. Testing is currently performed with 10 k Ω in the anode lead and 100 k Ω in the gate lead.

A single tip device, DOP1-1877-00-S12, operated at an average anode current greater than 1 μ A from October 4 to October 6 at a gate voltage of 200 V. This data is shown in Figure 4. The anode current was not terribly stable, but the gate current never rose above 10 nA, representing an emission efficiency of greater than 99.9%. After more than 24 hours of continuous bias, the device yielded the I-V curve shown in Figure 5.

Another single device from a different wafer, DOP1-0122-00-S14, operated under the same conditions at the same performance level for more than 24 hours. The device was disconnected and removed from the chamber to make room for RF testing. Data was not taken continuously on this device. MCNC capital has been applied to equipment that will allow data acquisition by computer, and plans are in place to implement automated DC data collection next quarter.

Continuous wave DC testing at relatively high current represents the most strenuous operation for field emitter devices. A 100% duty cycle allows no time for the device to cool. If the devices are operated with the gate electrode pulsed at 60 Hz, for example, the duty cycle is probably less than 10%. At this duty cycle, the array does not progress beyond its initial conditions. This does not realistically model the effect of gate heating from captured emission current, gate oxide leakage, and secondary and backscattered electrons from the anode that could be expected in a practical application, so much longer device lifetimes can be expected.

Silicon emitter array flat panel displays operate at even lower duty cycles. The resolution of a typical VGA display is 640x400, or 256,000 pixels. Even if the display is running continuously, each pixel is only active for 1/256,000 of the running time, regardless of the screen refresh rate. That represents a 0.0004% duty cycle, a much less demanding application of the technology.

1.2 Table 1 contains statistics on devices tested between July 30, 1993 and October 15, 1993. The table column titles denote observed device performance in the following way. "Working" means the device produced acceptable anode current at a gate voltage $V_g < 250$ V. "No emission" means either that no detectable gate or anode current was observed up to $V_g = 250$ V, or that the gate electrode shorted to the substrate while the device was under test. "Dead Short" means the gate electrode was shorted to the substrate prior to testing. Note that this data represents an average testing pace of 2.5 devices per workday.

1.3 High-frequency testing is performed in-house at MCNC and at the Litton subprogram site. In the original project timeline, it was intended that the Litton Solid State Division (LSSD) would mount the devices for testing by the Litton Electron Devices Division (LEDD). However, due to problems with previous test devices caused during packaging, it was decided that the devices would be packaged at MCNC. MCNC has mounted chips in holders produced by LSSD for LEDD to test.

The mounting method used by LSSD was to thin the wafers down to 100 μm , then scribe and break to separate the devices. Then, a AuSn eutectic die attach process is used to mount the chips to the holders after Ti/W-Au backside metal is applied to the thinned wafers. A small length of Al ribbon was used for the anode. This handling, plus their use of paraffin in the thinning process, destroyed the devices before they could be tested.

MCNC cut the arrays to size at full wafer thickness on a standard wafer dicing saw. The backside metal (Ti/Ni/Ag, described in the previous quarterly report) was applied prior to dicing, and the separate die were attached to the holders with SnAg solder paste. A small length of flat copper wire was used for the anode. The higher melting point of copper relative to aluminum, along with the increased thermal mass, should increase device performance.

The devices are tested in grounded-gate configuration, both at the Litton subprogram site and in-house. Grounded-gate operation tends to mask the gate-anode capacitance from the input, reducing unwanted bleedthrough of the input signal. Further, new anodes for the RF test fixtures have been fabricated from 0.010" thick copper foil with a stripe of Sn/Ag solder on one edge, and 2 μm of amorphous carbon evaporated over the surface. Although the amorphous carbon is not quite as conductive as crystalline graphite, it could have a similar effect on the measured gate current.

2.0 Device processing.

2.1 During the last quarter the processing of the field emitter runs continued. The first two runs of 2 μm column devices were completed and samples were prepared for electrical testing. The first wafer yielded good electrical performance as described in the previous quarterly report. From that wafer, several process parameters were evaluated to improve processing on later devices. The first variation that was investigated was a change in the gate metal thickness. This change enhanced the process by allowing removal of all the caps on a larger number of devices. It provided physical yield on the devices with the greatest number of tips (232,630). Several of these devices have been electrically tested, but so far have yielded no significant anode current before gate oxide failure.

Another process variation implemented as a result of the early electrical testing was the addition of a reoxidation sharpening step after all other device processing was complete. The statistical process integration analysis method attempts to correct for variation in each process step. In the case of the tip formation, the calculated etch target yielded tips with slightly larger radii than expected. The implementation of the reoxidation sharpening produced a much sharper tip at the end of the process. SEM inspection showed a reduction of measured tip radius from approximately 500 Å to below 200 Å.

The formation of the tip appears to be very important to the electrical performance of each array. For that reason, a second method of tip formation was also investigated as part of the first fabrication run. The standard process used to form the tips is the anisotropic crystallographic etch method. This forms a pyramid-shaped tip that can be oxidation sharpened later in the process. The second method forms round cone-shaped tips using an isotropic RIE silicon etch with SF₆. This process yielded extremely sharp tips with good current output and low turn-on voltage. However, tips formed with this method appear to exhibit less stable emission current than the pyramid tips.

Another metal system in addition to those described in the previous quarterly report was evaluated for the gate electrode in an attempt to eliminate the typical failure mode of the Ti / Pt system. A pure tungsten metalization scheme was used, but the film cracked due to the high stress inherent in the material. The devices still passed visual inspection, but electrical results on a tested device were poor.

The processing of the two 4 μ m column device lots has started. The formation of the larger column requires a thicker etch mask. This etch mask, along with other equipment related problems, caused major delays at the photolithography step in the processing of these runs. The difficulty was finally overcome by using the laser stepper, and the lots are proceeding in a timely fashion on a revised schedule.

2.2 One of the major challenges of producing large arrays of silicon emitter tips has been in producing a uniformly sized mask for the etching of the emitter tips themselves. This means producing large arrays of small circles with diameters on the order of 1 μ m. Since the tips are etched a whole wafer at a time, it means that uniformity must not only be good within each die, but good across the wafer as well. It also helps speed the processing if uniformity is good from wafer to wafer, since this allows batch processing of several wafers with the same process parameters.

It is also important that optimum uniformity be achieved at the lithography level, since the subsequent processing steps each add more non-uniformity. For this reason, extraordinary care has been taken with the initial lithography step to maximize uniformity. This extra care has caused delays in the processing of these lots.

Single wafer uniformity is determined by measuring 5 points within each of 5 die on the wafer, which takes from 20 to 30 minutes per wafer. After the data collection, the 25 measurement points are statistically analyzed. A three sigma variation of less than 0.1 μ m is expected. If this is not achieved, the data is analyzed again to see if variation is a function of location within each die, or absolute location of the measurement point on the wafer itself. If, for instance, there is variation within the die, but the same measurement point in each die is uniform with respect to the other four dice, a problem in focus or uniformity of the light field is most likely. On the 2 μ m column device runs, the initial lithography showed very good uniformity from one wafer to the other for the same absolute location on the wafer, but poor uniformity within the wafer. This was traced to particles and other anomalies on the chuck surface, which required an aggressive cleaning procedure to produce acceptable uniformity.

One factor that militates against succeeding in this uniformity is that the circles that are imaged have a diameter that is on the order of the resolution of the system. Imaging of

features this size is especially sensitive to lens aberrations. If focus is not optimum, astigmatism in the lens will cause the circle to become an ellipse. If the major concern is lines that are horizontal and vertical, this astigmatism might be unnoticeable, depending on the orientation of the elliptical axes. In the small circles that define the emitter tips, it means that at one point, the "diameter" is significantly less than the mean. In evaluating uniformity, one must not only look at the measurement numbers, but make an assessment of how good the circularity of the circles measured is.

In the processing of these lots, good uniformity was achieved on the first two fabrication runs of 2 μm column devices, but only after some extensive troubleshooting and analysis. These are device quality wafers with a pad oxide and nitride layer, which were then coated with photoresist and exposed with our I-line stepper. Since the oxide and nitride layers are extremely uniform, once the anomalies on the stepper chuck were corrected, good uniformity was achieved without the need for an antireflective coating. The first device produced wafers with excellent electrical test results, so there does seem to be some correlation between good emission characteristics and lithographic uniformity.

In the third and fourth runs (4 μm column devices), repeated attempts were made to achieve the same uniformity on the I-line stepper with no success. The only difference in the process flow of these lots is that in addition to the oxide and nitride, there is a layer of Low Temperature Oxide (LTO), which is necessary to form the taller column structures. It may be that this LTO layer adds some non-uniformity to the wafers that either caused variations in reflectivity across the wafer, or might have confused the automatic focus system. Delays were aggravated by about 3 weeks of mechanical and electrical problems with the I-line stepper.

These problems and delays prompted a decision to use the laser stepper for the initial lithography step on the 4 μm column device runs. This is a more expensive process that requires several modifications for acceptable performance with field emitter devices. First, "detuning" of the laser is required, since it is normally optimized for resolution and not uniformity. With the correct detuning, astigmatism at the edges of the field will be minimized. Also, due to the smaller wavelength of the laser (248 nm) an anti-reflective coating is required in addition to the standard photoresist. This adds another coating step and another etch step, which again militates against uniformity, but it was hoped the gains would outweigh the losses. This proved to be the case, as on the first 4 μm device run variation was just over 0.1 μm across the lot.

In summary, the delays in the processing of these lots are due in part to the need for unusually high uniformity on a non-standard structure, as opposed to typical CMOS processing. This requirement revealed new photolithography problems and challenges that have yet to be resolved. Delays were also aggravated by equipment problems. It does appear, however, that the unprecedented success in testing shows the effort was worthwhile.

3.0 Vacuum testing and microencapsulation bonding system.

3.1 An *in-situ* plasma cleaning system was installed and evaluated in the test chamber. The system uses forming gas, a non-flammable mixture of 10% hydrogen and 90% nitrogen, rather than pure hydrogen, for safety reasons. The system uses equipment and supplies that were available in-house at no additional cost to the

contract. However, installation of this system delayed completion of the whole-wafer test system installation.

The substrate of the device serves as one electrode. To minimize the number of electrical feedthroughs required, the other electrode is the anode used for emission testing. In the current test configuration, the anode is about 2 mm from the device in DC testing, and about 5 mm in high-frequency testing. The anode power supply provides adequate voltage and current to strike a plasma.

The system operated well on first attempt. A plasma was applied to the test devices for 5 minutes at 60 mTorr. After the cleaning, no current output was observed. On visual inspection of the devices, it was noted that the gate electrodes were destroyed on the devices that were wirebonded. In a sense, this is not surprising. Since only the ones that were wirebonded blew out, the wirebonds and connecting wires may be acting as antennas and charging the gate electrodes to a high voltage. If the test leads are connected to ground, the charge has an easier leakage path to ground than an arc to the emitter tips. Subsequent experiments used shorter plasma cleaning times, but the same device destruction was observed. A literature search on results from other experimenters is being conducted in an attempt to identify and solve the problem.

3.2 One micromanipulator was installed on the test chamber. The quartz insulators for the whole-wafer test stage have been installed. Design of the metal parts for the test stage is being completed. Fabrication and installation is expected to be complete in the next quarter.

4.0 Other Developments.

4.1 Development of low work function and metal coatings is proceeding well. The work in the present review period has been focused on the optimization of the deposition process for tantalum nitride, TaN (reported work function value ϕ of 1.9 eV), and on the development of deposition processes for lanthanum hexaboride, LaB₆ ($\phi \approx 2.7$ eV) and zirconium carbide, ZrC ($\phi \approx 2.2$ eV).

4.1.1 TaN films.

Investigated TaN films are obtained via reactive sputtering of Ta in a nitrogen atmosphere in a Perkin-Elmer 4450 RF Sputtering System located in the MCNC's clean room facility. As a result of the present study, the following process conditions have been identified for deposition of stoichiometric TaN:

- rf power of 1.5 kW,
- partial pressure of N₂ of $3.5 \cdot 10^{-3}$ Torr,
- total pressure of $6.0 \cdot 10^{-3}$ Torr.

The chemical composition of the sputtered films have been analyzed by means of Auger Electron Spectroscopy (AES) and X-Ray Diffraction (XRD). Figure 6 shows the XRD spectrum for a 4000 Å thick film deposited under the conditions specified above. The position and relative magnitude of the peaks in the spectrum are as expected for fcc TaN (a face centered cubic crystallographic structure). The investigated TaN films adhere well to silicon, and have resistivity of 210 - 220 $\mu\Omega \cdot \text{cm}$. The film growth rate is 1 Å per second.

As a first step in the integration of the coating into silicon emitter devices, a thin (< 200 Å) TaN film was deposited on ungated silicon emitter structures. Figures 7a and 7b show SEM micrographs of the emitter structures prior to the coating step and after the coating step, respectively. The deposition appears to be conformal and the geometrical structure of the emitter tip is not changed appreciably. The ungated TaN coated devices will be tested electrically in a diode configuration and the results will be compared with electrical data for ungated uncoated silicon emitters.

4.1.2 LaB₆ films.

As a part of the present study, we have been developing a process for deposition of thin films of LaB₆. Since LaB₆ is expected to evaporate congruently in the vicinity of its melting point, e-beam evaporation was chosen as a means of the film formation. The source material in the form of 99.5 % pure LaB₆ pellets has been purchased from CERAC, Inc. The e-beam evaporation has been performed in the BAK 760 system located in the MCNC's clean room facility.

The chemical composition of evaporated films has been examined using AES and X-Ray Photoelectron Spectroscopy. A pellet of the source material has been used as a reference in the analyses. The AES spectra indicated that the ratio of B to La in the bulk of the film is close to the expected value of six. This result was confirmed by the XPS analysis, which in addition provided information about chemical bonding of elements present in the films, both with regard to the surface and the to bulk of the film. The evaporated films adhere well to silicon, and have resistivity of $5.6 \text{ m}\Omega\text{-cm}$. The film growth rate is 5 Å per second .

The plans for the next review period include depositing a thin LaB₆ coating on ungated silicon emitters and electrical testing of the coated structures in a diode configuration. In a parallel manner, the integration of the LaB₆ coating into gated silicon field emitter devices will be investigated. Since the LaB₆ evaporation takes place under a low background pressure ($5 \cdot 10^{-6}$ Torr), it is expected that the film will be deposited only on silicon emitters, and not on the sidewalls of the interelectrode insulator, which is shadowed during the deposition process by the gate metal. If this is the case, the coating step could be performed at the very end of the device process flow.

4.1.3 ZrC films.

Initial test runs have been performed to test the feasibility of obtaining thin ZrC coatings by means of an e-beam evaporation technique. The 99.5% pure pellets of ZrC have been obtained from CERAC, Inc. After initial optimization of the process, the evaporation resulted in a deposition of mirror-smooth well-adhering films with a resistivity of $3.1 \text{ m}\Omega\text{-cm}$. The film growth rate is 10 Å per second . The films were analyzed by AES. The AES spectra have been compared with spectra obtained from the source material. The Zr to C ratio in the film is equal (within the experimental error of the method) to that of the source.

As in the case of LaB₆, integration of the ZrC coatings into the process sequence for ungated and gated silicon emitters will be investigated.

4.2 A device serialization method was implemented to improve record keeping on field emitter device testing. The serial number format LLLL-WWRC-PP-DD is used, with the meaning of each letter shown in Table 2. Following the convention of MCNC's primary inspection tool, the Hitachi S6000 SEM, with the primary flat of the wafer down, the die are arranged on the wafer in rows and columns as shown in Figure 8. Note that the row and column numbers start with 0 rather than 1. In each die, there are several sections as described in the mask design section of the previous quarterly report. The devices in each section are designated as shown in Table 3.

Using this system, the serial number for a 6 μm pitch ARPA array from row 1 (the second row) column 3 (the fourth column) of fabrication run DOP1, wafer number 18, would be

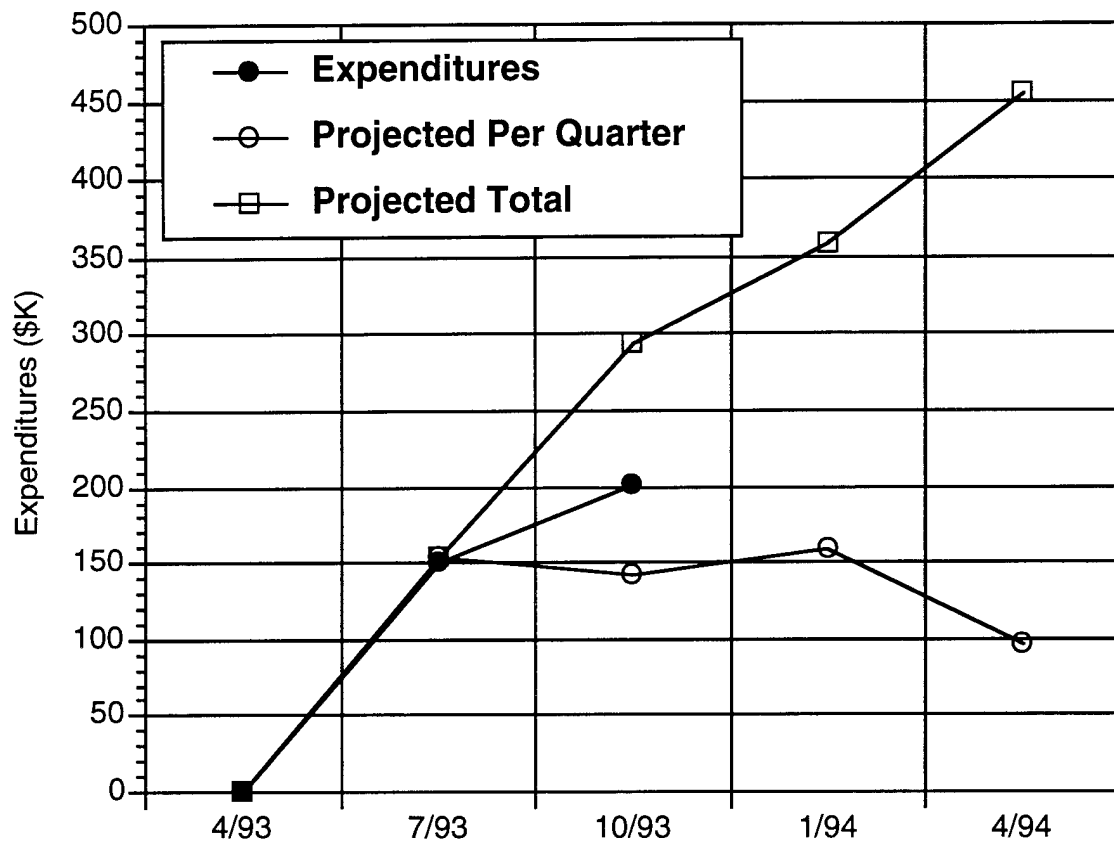
DOP1-1813-06-A?

where the ? is replaced by the number of the particular array under test.

4.3 Theoretical calculations of the emission area and field enhancement factors for field emitter arrays were made using data collected from devices tested at MCNC. The work function of the silicon tips was assumed to be 4.50 eV. The results of the calculations are shown in Table 4.

The emission area does not scale linearly with the number of tips. This indicated that the tips are not all of the same radius, but follow some distribution. From these results, it appears that the vast majority of the emission current originates from the tips with the smallest tip radii, even though they comprise only about 0.3% of the total number of tips. The slope of the Fowler-Nordheim plot of the data gives a field enhancement factor only 5% lower than the field enhancement factor of the smallest tips. This would indicate that, using reasonable assumptions, we can model the electrical performance of the devices using the Fowler-Nordheim equation with statistical data on, or a reasonable assumption about, the tip radius distribution. It also underlines the importance of the tip radius on the emission current.

IV. Fiscal Status



Expenditures this quarter (7/16/93 - 10/15/93)	\$49,890.64
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Total expenditures to date (4/16/93 - 10/15/93)	200,623.33
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Contract Amount (Option 1)	\$454,965.00
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Note: Quarterly expenditures are based on financial data and contract commitments through 9/28/93 and estimated processing costs through 10/15/93. The difference between projected and actual spending is largely due to processing delays which push costs into the next quarter. Subcontract billing was expected to occur in this quarter as well, but is now scheduled for next quarter.

V. Problem Areas

The successful electrical performance of the recently fabricated silicon based field emitter arrays opens a new door to quality control and reliability issues. The initial development stage leads to devices that at some point in the electrical testing, fail. In order to secure the most reliable electrical part, the modes for these failures must be addressed. The failure modes of these microstructures are being analyzed by destructive construction analysis.

Tested devices that yield high currents are examined post-test using an optical microscope to assess damage to the structure. The main failure mode that is exhibited is the destruction of the Ti/Pt gate metal leading to short circuits between the gate electrode and substrate. This phenomenon is observed in nearly all the field emitter arrays that emit significant current. Examination of the devices using scanning electron microscopy is the next step. This has identified one problem in the fabrication method. There is a significant amount of undercut of the gate metal at the cap removal step. This has been identified as a possible cause for the gate metal shorting for the following reason. The insufficient support of the gate metal surrounding the field emitter tip may allow the gate metal to bend when subjected to electrostatic forces caused by the gate potential. When the electrode bends close to the emitter, the spacing could allow an arc to form, causing the destruction of the gate metal at that tip location. Several solutions have been proposed and are under investigation.

The destruction of the gate metal may also be due to arcing caused by high local pressure when the devices heat up during operation, causing out-gassing of the gate oxide and other structural components. Heating the devices directly during the pumpdown and bakeout of the chamber may reduce the amount of gas trapped in the surface of the oxide.

The final yield inhibiting failure identified so far is related to the cap removal step. As discussed previously, the caps are removed and the oxide etched away to form a cavity with the field emitter tip in the center of the opening. It has been determined that during the gate metal deposition, the metal is migrating past the caps and into the cavity surrounding the emitter, causing the cavity formation to be inhibited and possibly leading to gate to emitter shorts. This failure mode is under examination, and subsequent device fabrication runs will include processing adjustments to solve the problem.

VI. Visits and Technical Presentations

Weekly closed meetings were held between MCNC staff and its subcontractors. A field emitter DC test procedure review with MCNC personnel external to the program was held on August 19, 1993. The purpose of this review was to obtain an objective evaluation of the field emitter test procedures from experienced members of the technical staff not intimately familiar with the program. One meeting was held with personnel outside the direct program participants on July 19, 1993. This person was Professor Jong Duk Lee from Seoul National University. Dr. Lee presented a seminar at MCNC on a new recessed gate MOSFET, then met with the field emitter group for one hour for an exchange of general ideas on field emission.

The extended abstract of the poster session entitled "Field Emitter Array Process Optimization and Performance Prediction", presented at the International Vacuum Microelectronics Conference in Newport, Rhode Island July 12-15 1993, will be included in the conference proceedings. One staff member attended the 184th Meeting of the Electrochemical Society, October 10-15 in New Orleans, and presented a talk entitled "Fabrication of Uncoated and Coated Silicon Field Emitter Arrays". The slides from this presentation are included as Attachment A. This presentation is being rewritten as a paper, intended for publication in the Journal of the Electrochemical Society. An abstract, tentatively titled "Large Arrays of Gated Silicon Field Emitters as High-Intensity Electron Beam Sources", is being prepared for submission to the 1994 Tri-Service/NASA Cathode Workshop in Cleveland, Ohio March 29-31 1994. A paper detailing MCNC's DC test results, tentatively titled "DC Performance of Large Arrays of Silicon Field Emitters", is in preparation for submission to the IEEE Transactions on Electron Devices.

DOP1-1823-06-Q4 TEST 1

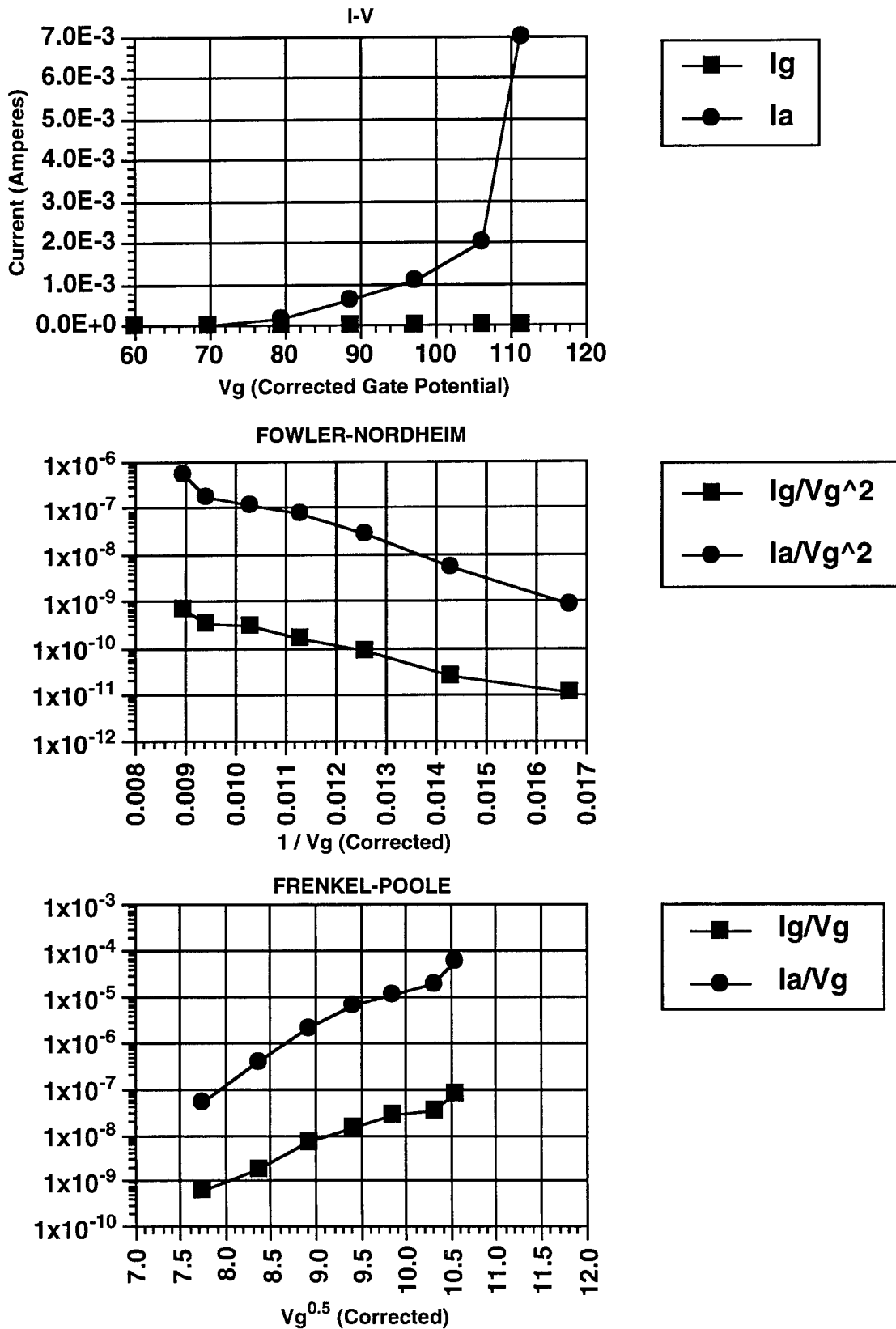


Figure 1: Data from 44,460 tip array plotted with corrected gate potential.

DOP1-2323-10-L3

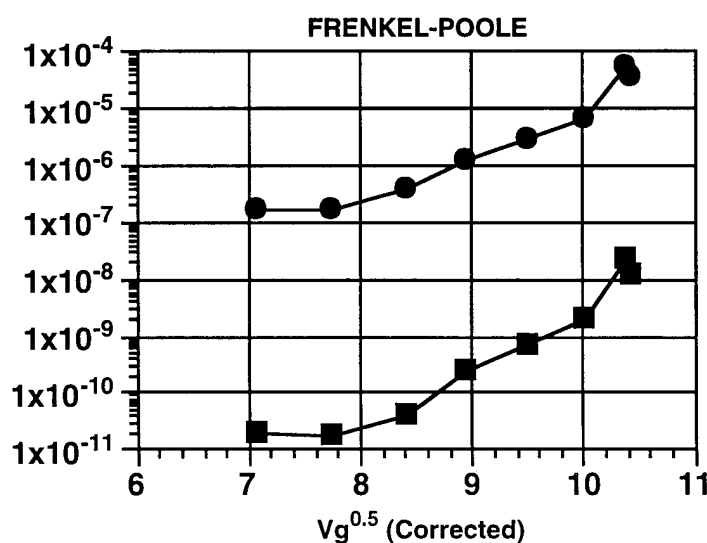
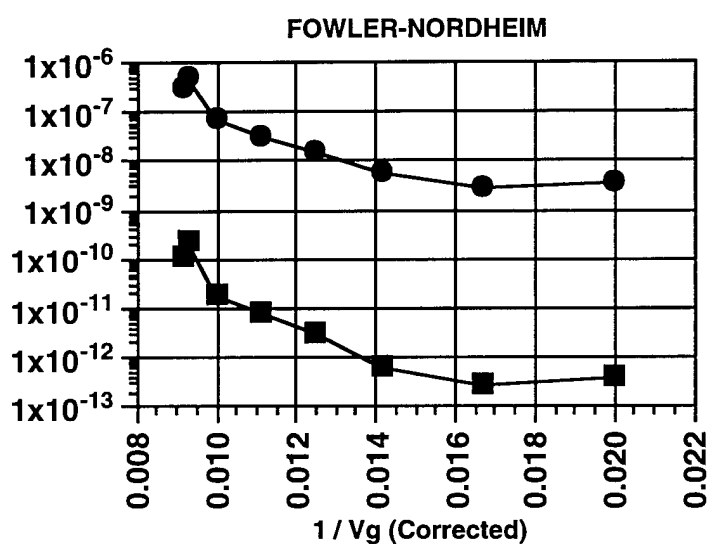
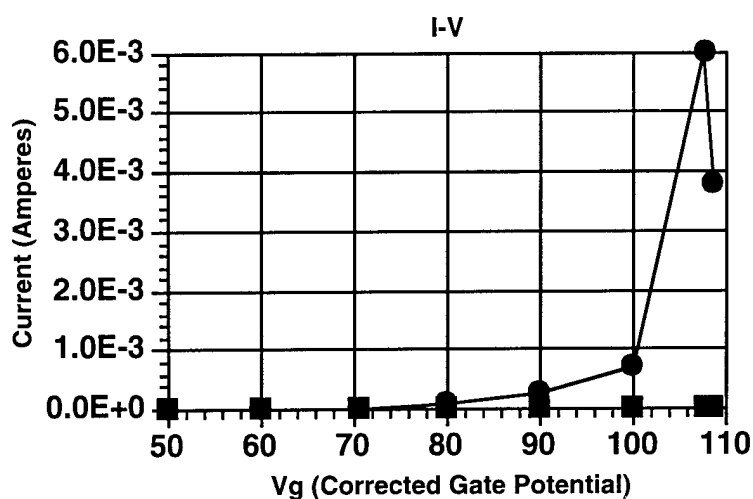


Figure 2: Data from 6,648 tip array plotted with corrected gate potential.

DOP1-2323-10-A5

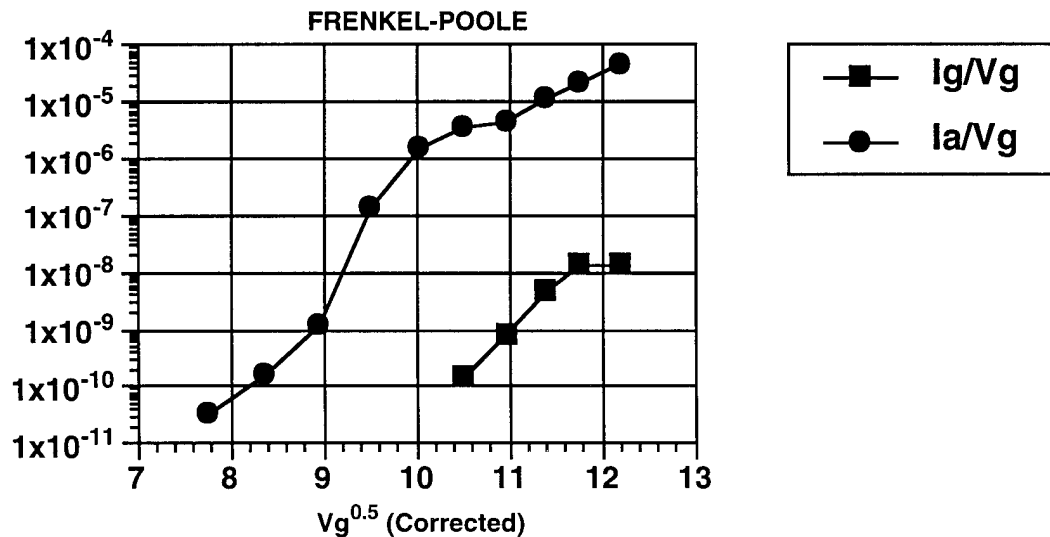
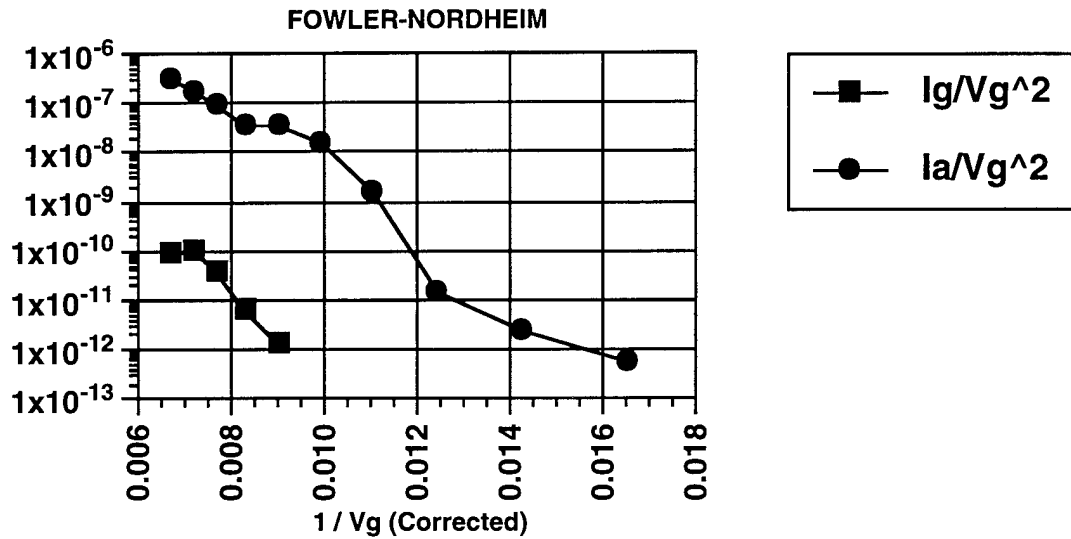
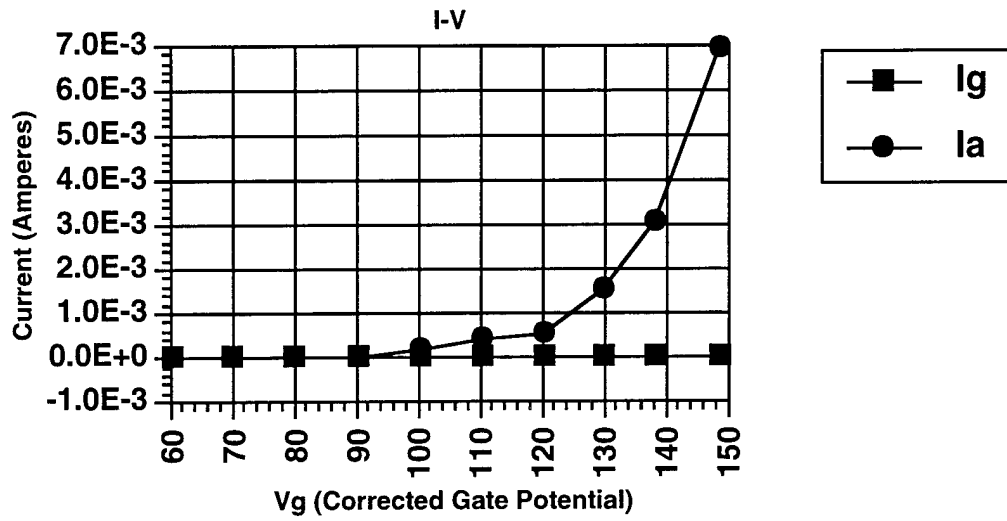


Figure 3: Data from 1,192 tip array plotted with corrected gate potential.

DOP1-1877-00-S12
 Tested from 5 OCT 93 to 7 OCT 93

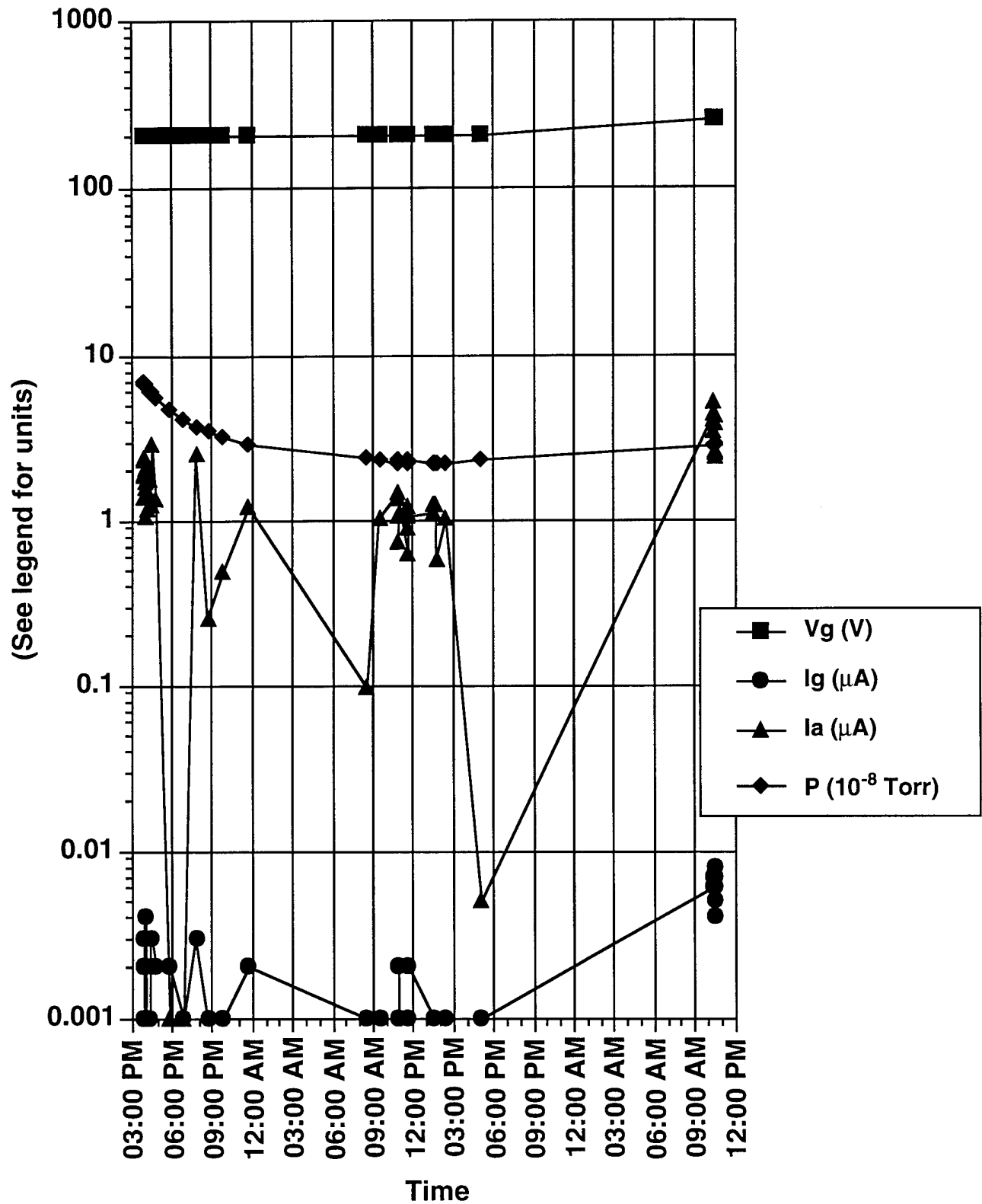


Figure 4: Lifetime test for a single tip device.

DOP1-1877-00-S12

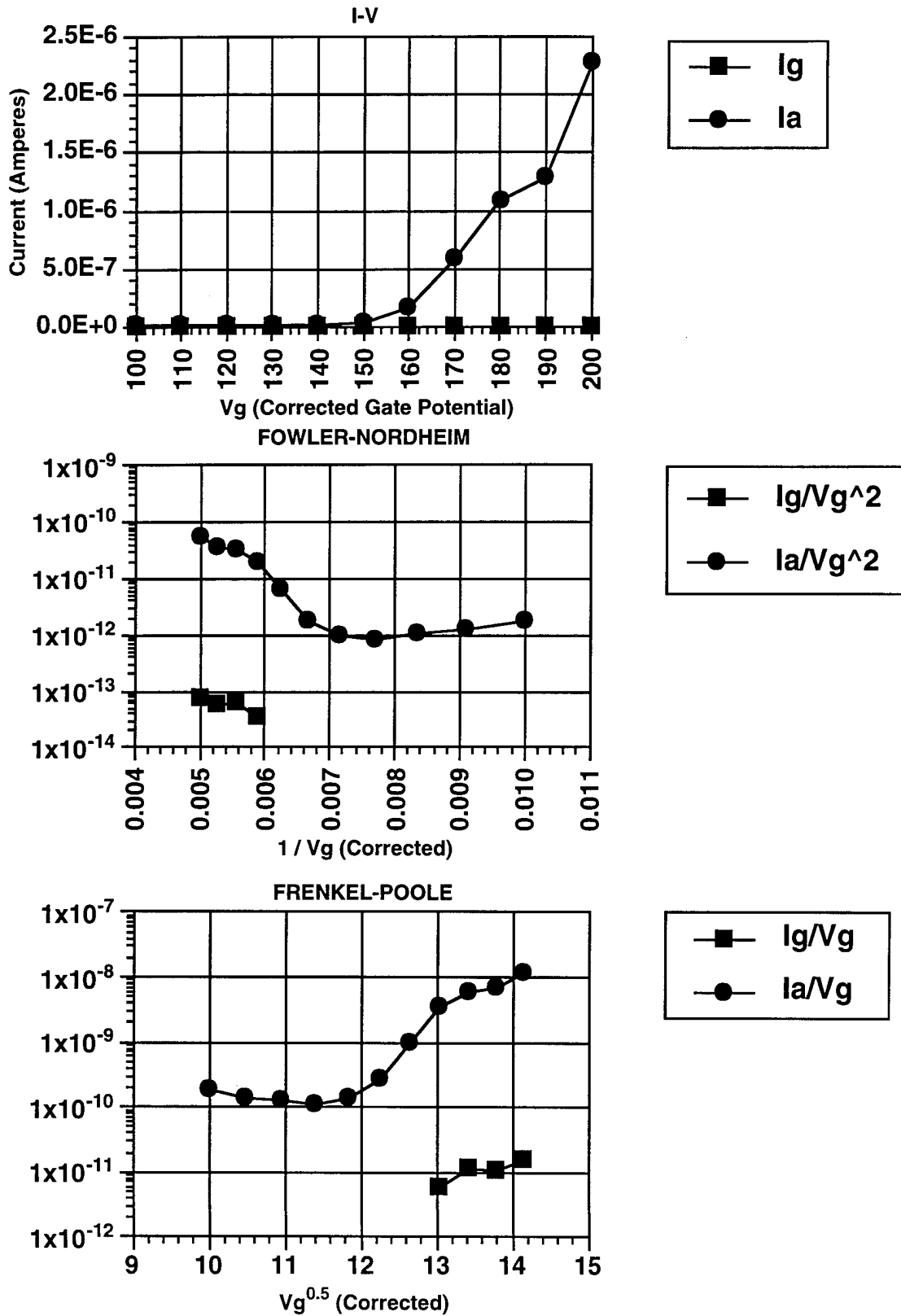


Figure 5: Measured data from device in Figure 4 after 24 hour operation.

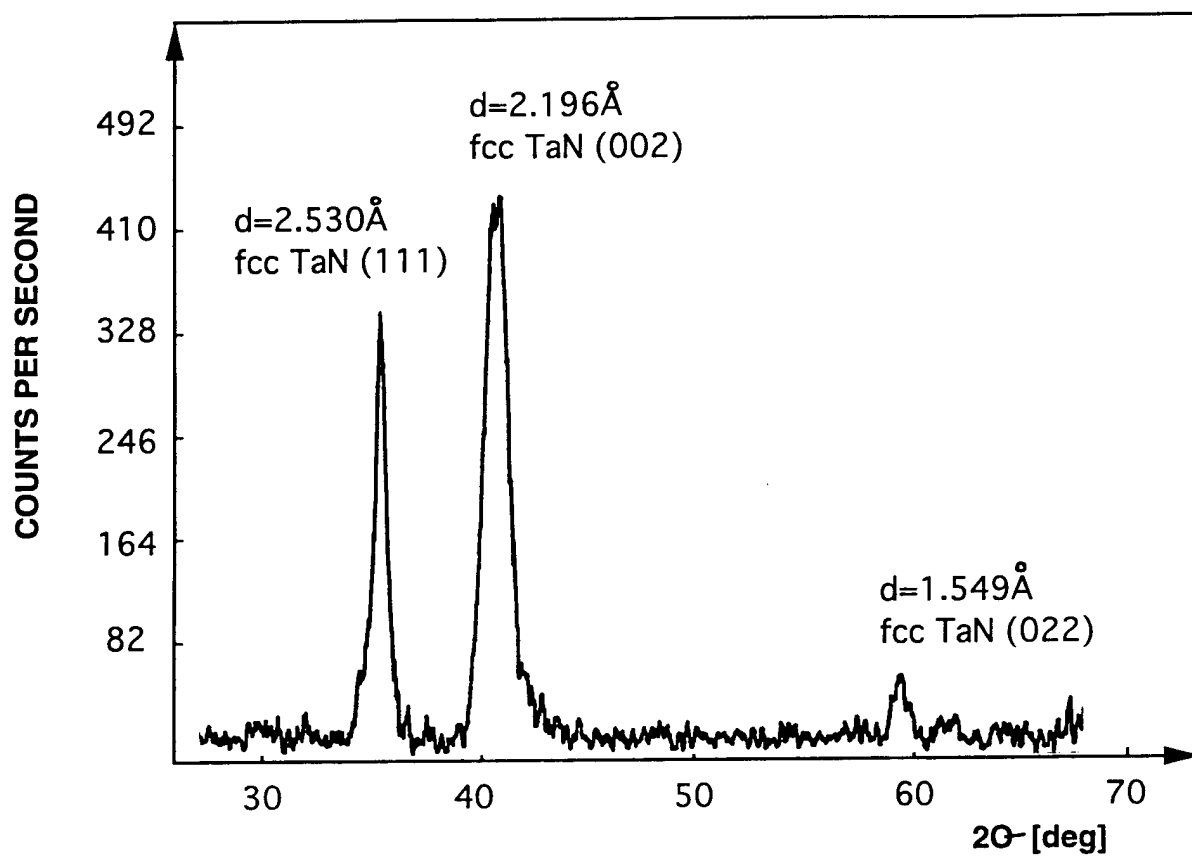


Figure 6: X-ray diffractogram of a thin TaN film obtained by RF reactive sputtering of Ta in an N_2/Ar ambient.

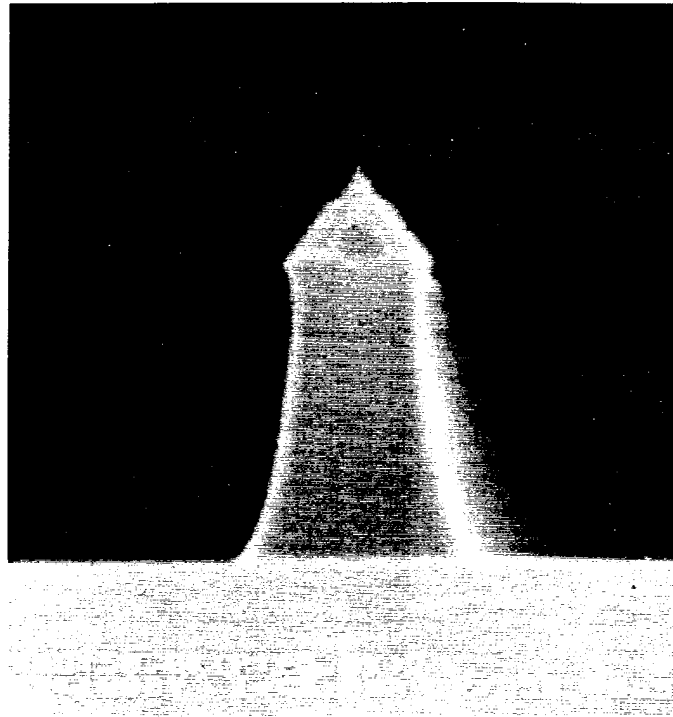


Figure 7a: SEM micrograph of silicon emitter structures prior to coating.

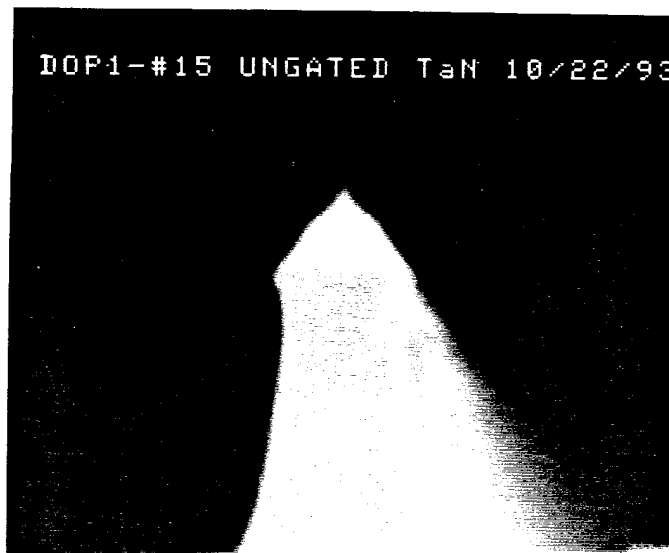


Figure 7b: Emitter structures after coating with a thin ($< 200 \text{ \AA}$) TaN film.

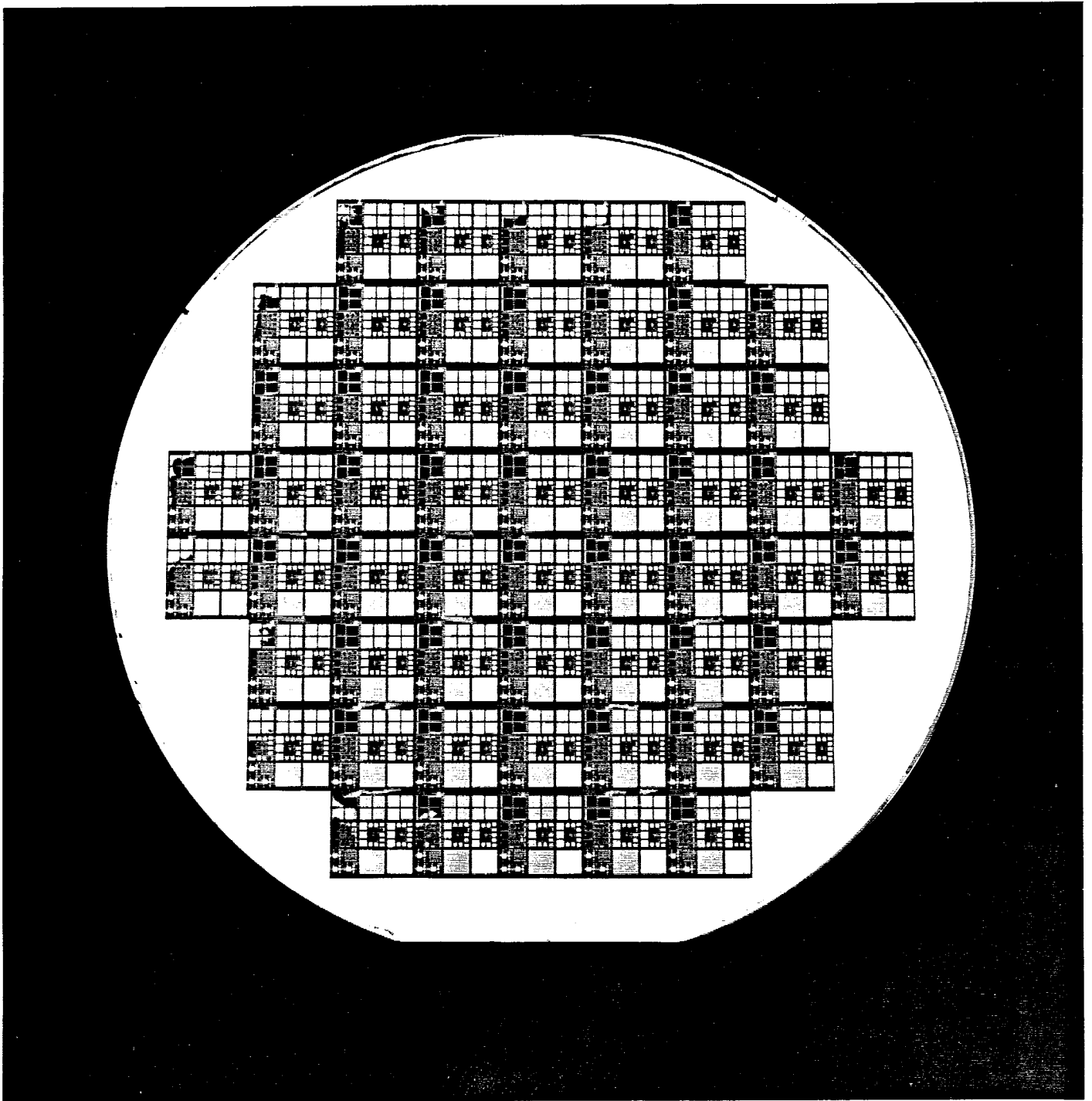


Figure 8: Option 1 device wafer.

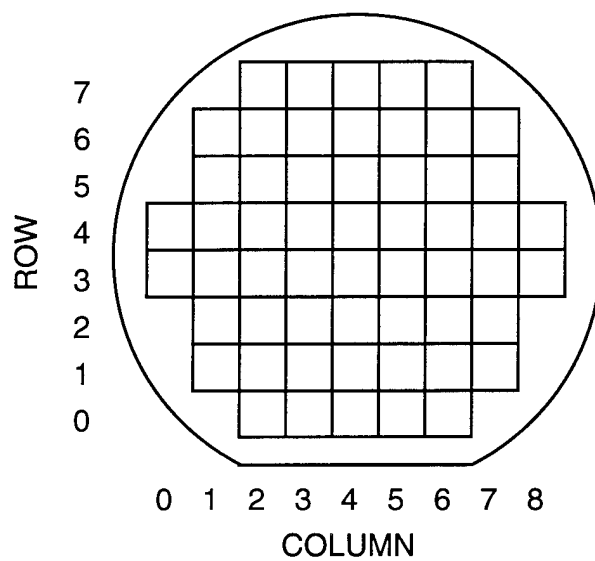


Figure 9: Option 1 device wafer map.

Array Type	Tested	Working	No Emission	Gate Short
ARPA 4 μm	10	3	0	7
6 μm	48	22	10	17
10 μm	24	21	2	1
Litton 4 μm	0	0	0	0
6 μm	13	0	1	12
10 μm	5	5	0	0
Quad 4 μm	0	0	0	0
6 μm	4	3	0	1
10 μm	4	0	0	4
Huge 6 μm	1	0	0	1
10 μm	0	0	0	0
Single Tip	27	7	20	0
10x10 4 μm	1	1	0	0
6 μm	1	1	0	0
10 μm	1	0	0	1
5x5 4 μm	0	0	0	0
6 μm	0	0	0	0
10 μm	0	0	0	0
4x4 4 μm	0	0	0	0
6 μm	0	0	0	0
10 μm	0	0	0	0
3x3 4 μm	0	0	0	0
6 μm	0	0	0	0
10 μm	0	0	0	0
2x2 4 μm	0	0	0	0
6 μm	0	0	0	0
10 μm	0	0	0	0
Total	139	63	33	43
Percent		45	24	31

Table 1: DC test program statistics covering the time period
from July 30, 1993 to October 15, 1993

LLLL	Lot name (DOP1-DOP6)
WW	Wafer number (typically 01-50)
R	Die row number
C	Die column number
PP	Pitch of the tips in microns (04, 06, or 10)
DD	Device number

Table 2: Definition of device serial number using the format LLLL-WWRC-PP-DD.

ARPA	A1 - A9, clockwise from top left
Huge	H or HH, there is only one per tip pitch
Litton	L1 - L3, top to bottom
Quad	Q1 - Q4, clockwise from top left
Single tips	S1 - S16, counter-clockwise from top right
eXperimental	X1, X2, X3, X4, X5, XX where XX is the
	10 x 10 array

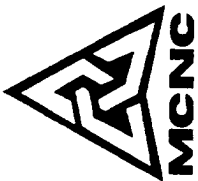
Table 3: Device designation for serial numbers.

DEVICE NUMBER	ϕ (eV)	β ($\times 10^4$ V/cm)	Emission area (cm^2)	Number of tips
DOP1-1814-04-XX	4.50	92.0	$1.227 \cdot 10^{-14}$	100
DOP1-1814-06-XX	4.50	54.1	$10.48 \cdot 10^{-14}$	100
DOP1-0841-06-A8	4.50	44.6	$62.13 \cdot 10^{-12}$	3255
DOP1-0841-06-A7	4.50	36.1	$74.53 \cdot 10^{-12}$	3255
DOP1-0841-06-A6	4.50	46.0	$73.66 \cdot 10^{-12}$	3255
DOP1-0841-06-A3	4.50	56.1	$8.71 \cdot 10^{-12}$	3255
DOP1-1814-10-L3a	4.50	69.0	$7.77 \cdot 10^{-12}$	6648
DOP1-1814-10-L3b	4.50	77.1	$1.31 \cdot 10^{-12}$	6648
DOP1-1814-00-S4a	4.50	57.0	$2.390 \cdot 10^{-14}$	1
DOP1-1814-00-S4b	4.50	29.8	$22.07 \cdot 10^{-14}$	1
DOP1-1814-00-S4c	4.50	27.1	$8.360 \cdot 10^{-14}$	1

Table 4: Theoretical calculations of field enhancement factor and emission area using measured DC performance data.

LIST OF ATTACHMENTS

Attachment A: "Fabrication of Uncoated and Coated Silicon Field Emitter Arrays", 14 pages.

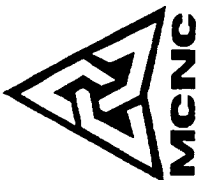


FABRICATION OF UNCOATED AND COATED SILICON FIELD EMITTER ARRAYS

C.A. BALL, F.F. LEE, X. LIU, G.E.MCGUIRE,
W.D. PALMER, D. TEMPLE, D.G. VELLENGA AND L. YADON

MCNC
ELECTRONIC TECHNOLOGIES DIV.
RESEARCH TRIANGLE PARK, NC 27709-2889

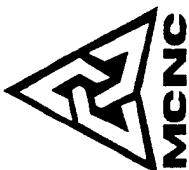
THE WORK HAS BEEN SUPPORTED IN PART BY ARPA CONTRACT
NUMBER MDA972-91-C-0028.



ACKNOWLEDGEMENTS

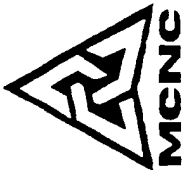
THE AUTHORS WOULD LIKE TO ACKNOWLEDGE CONTRIBUTIONS
OF AND VALUABLE DISCUSSIONS WITH:

- JOE MANCUSI OF DUKE UNIVERSITY,
- MARK KELLAM and KEN WILLIAMS OF MCNC,
- ARNOLD REISMAN OF NCSU,
- HENRY GRAY and JONATHAN SHAW OF NRL.



OUTLINE

- INTRODUCTION - FIELD EMITTER FABRICATION AT MCNC
- FIELD EMITTER STRUCTURE GEOMETRY VS. DEVICE PERFORMANCE - SIMULATION
- PROCESS FLOW FOR GATED FIELD EMITTER
- STATISTICAL PROCESS INTEGRATION ANALYSIS IN FABRICATION OF LARGE ARRAYS
- DC ELECTRICAL PERFORMANCE OF SINGLE EMITTERS AND EMITTER ARRAYS
- DEVELOPMENT OF DEPOSITION PROCESSES FOR LOW WORK FUNCTION EMITTER COATINGS
- SUMMARY

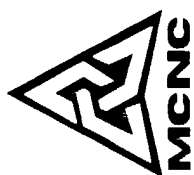


FIELD EMITTER FABRICATION AT MCNC

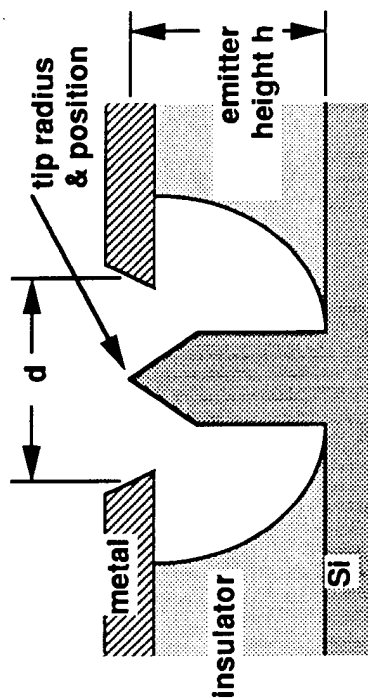
- SILICON BASED TECHNOLOGY - DRAWING FROM THE IC EXPERIENCE
- FOCUS ON HIGH PERFORMANCE GATED FIELD EMITTER ARRAYS (FOR e.g. EMISSION GATED RF AMPLIFIERS)

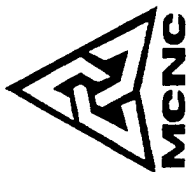
PERFORMANCE REQUIREMENTS:

- * TOTAL EMISSION CURRENT: mA RANGE
 - * GATE VOLTAGE: <250 V
 - * CURRENT DENSITY: A/cm² RANGE
 - * OPERATIONAL AT GHz FREQUENCIES
- FIGURE OF MERIT: $fT = g_m/2\pi C$

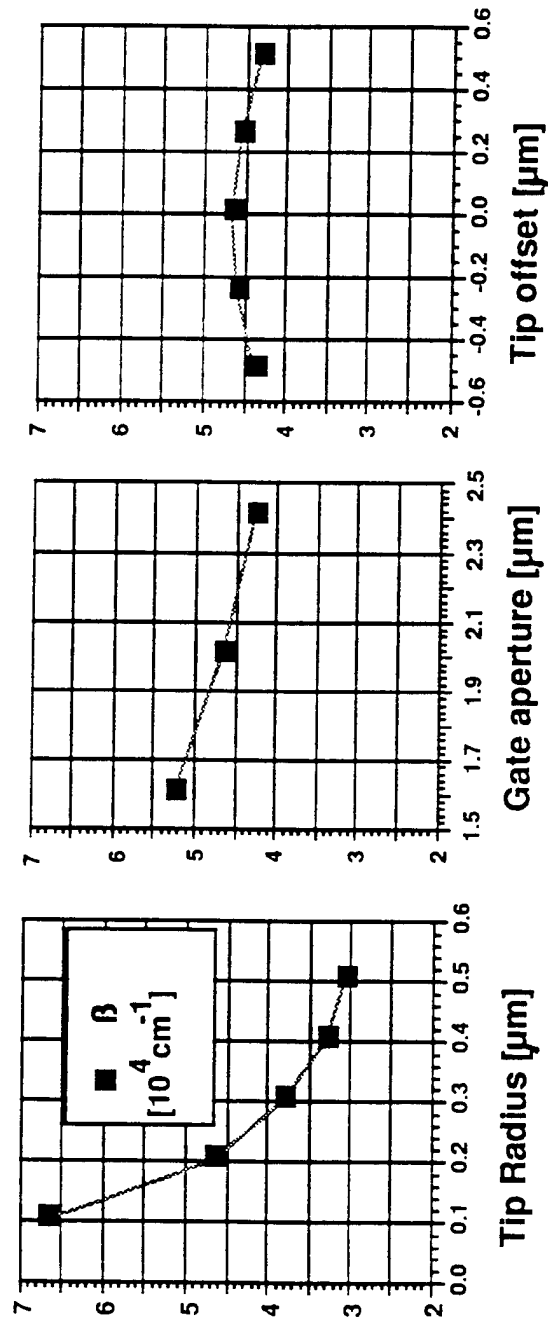


COLUMN EMITTER GEOMETRY



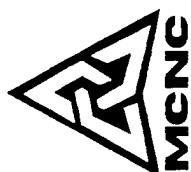


SIMULATION - EFFECT OF GEOMETRY ON FIELD ENHANCEMENT FACTOR



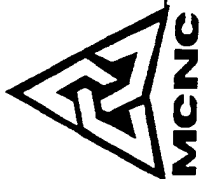
$$E = \beta V_g$$

$$I/Vg^2 = A (\text{const } \beta^2 / \phi) \exp(-\text{const } \phi^{1.5} / \beta / V_g)$$

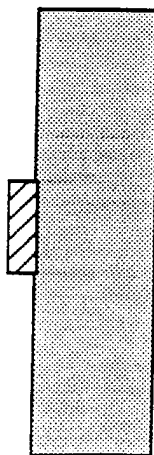


PROCESSING OBJECTIVES

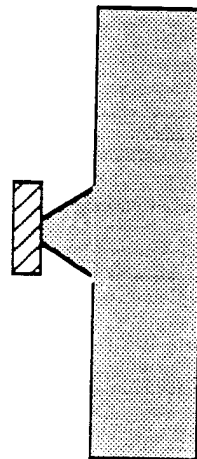
- UNIFORMLY SHARP TIPS
- TIPS CENTERED VERTICALLY IN GATE METAL
- MINIMUM GATE APERTURE DIAMETER
- YIELD ON LARGE ARRAYS



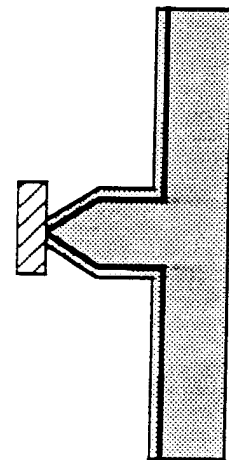
SELF ALIGNED FIELD EMITTER STRUCTURE



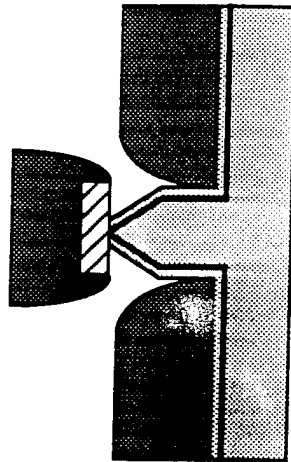
Deposit insulator and pattern



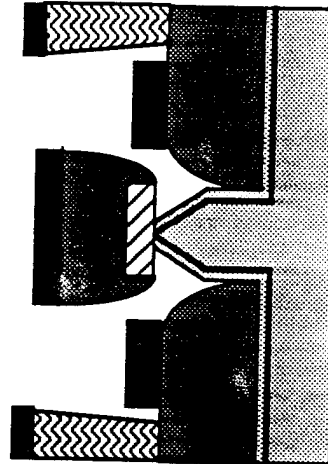
Anisotropic etch to form pyramids



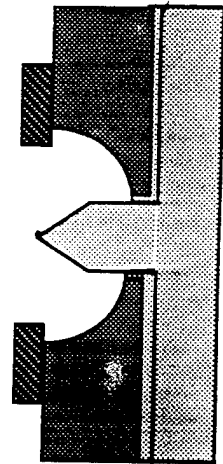
Etch columns and sharpen tips(oxidation)



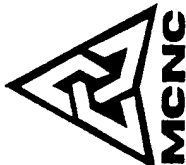
Evaporate insulator



Pattern photoresist & deposit metal

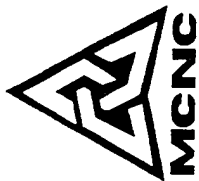


Lift metal and etch insulator

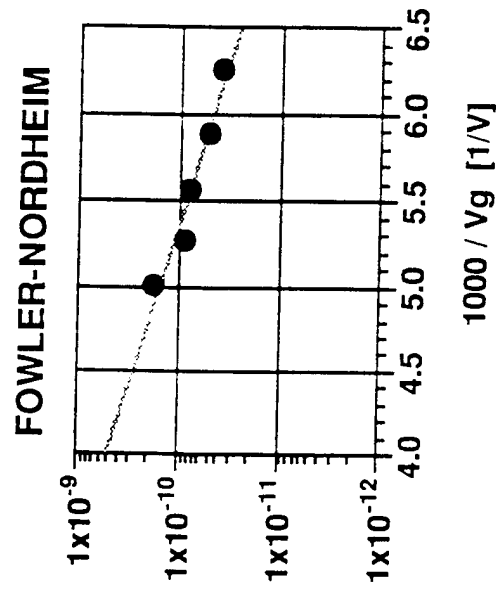
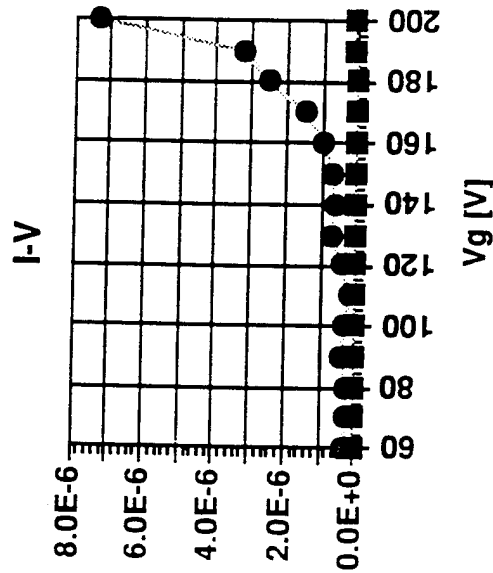


STATISTICAL PROCESS INTEGRATION ANALYSIS

- GATHER DATA ON STATISTICAL DISTRIBUTION OF PROCESSING PARAMETERS IN EACH STEP (E.G. DISTRIBUTION OF ETCH MASK DIAMETER)
- USE PROCESS VARIATIONS AND KNOWN DIMENSIONAL LIMITS TO CHOOSE PROCESSING TARGETS (E.G. THICKNESS OF SILICON TO BE ETCHED IN PYRAMID FORMATION)
- PREDICT FINAL DISTRIBUTIONS OF GEOMETRICAL PARAMETERS OF DEVICE STRUCTURE (E.G. EMITTER HEIGHT DISTRIBUTION)

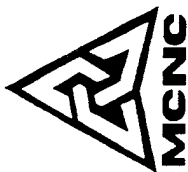


ELECTRICAL PERFORMANCE - SINGLE EMITTER

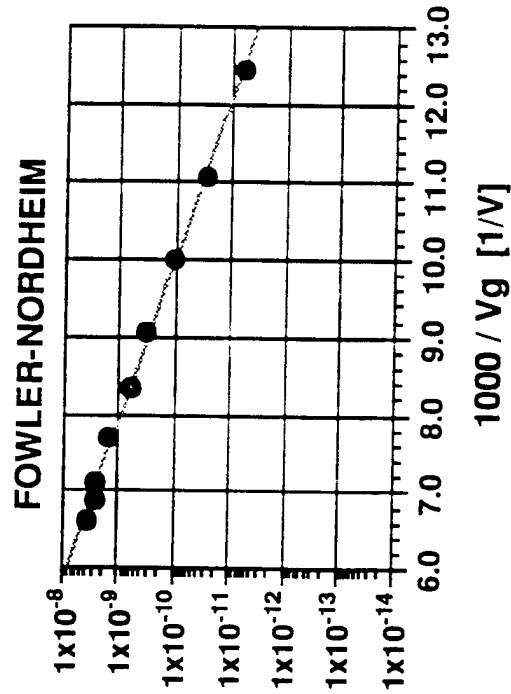
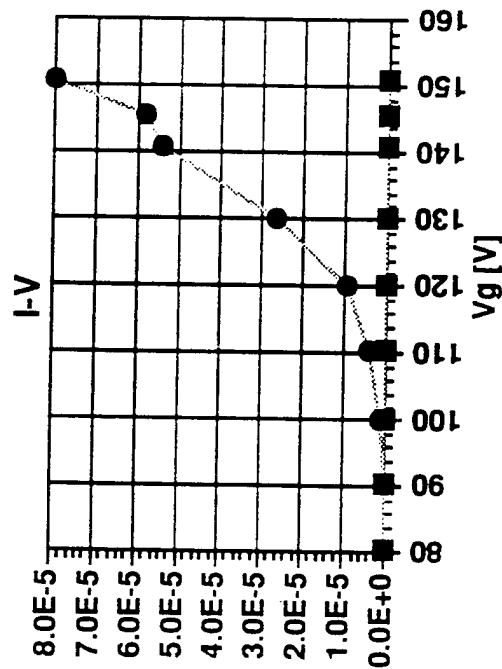


$$I/Vg^2 = 5.88E-8 * \exp(-1190/Vg)$$

$$R^2 = 0.940$$

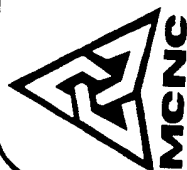


ELECTRICAL PERFORMANCE - 10X10 ARRAY

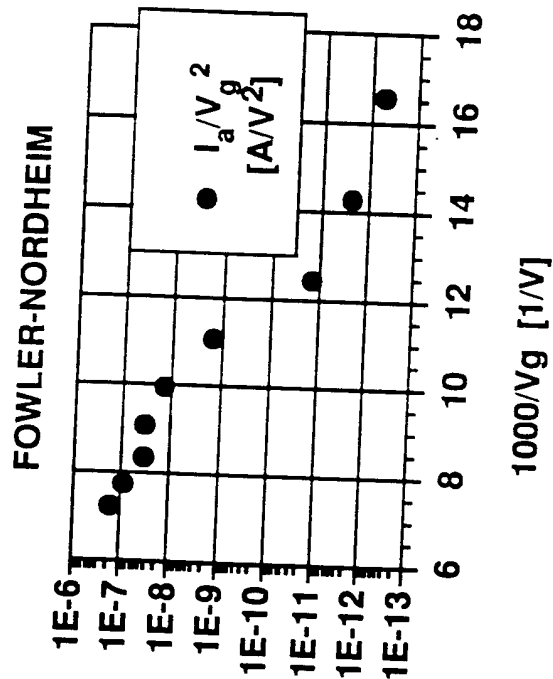
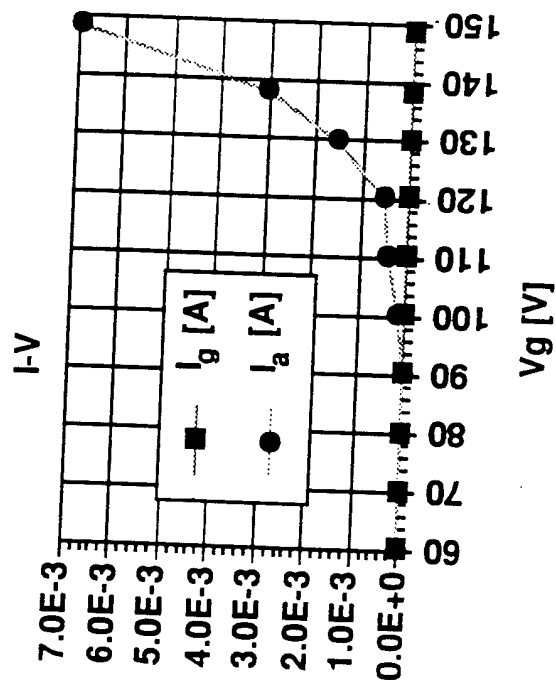


$$I/V_g^2 = 6.54E-6 * \exp(-1110/V_g)$$

$$R^2 = 0.996$$

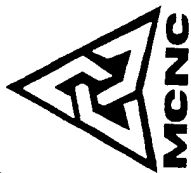


ELECTRICAL PERFORMANCE - 1197 TIP ARRAY

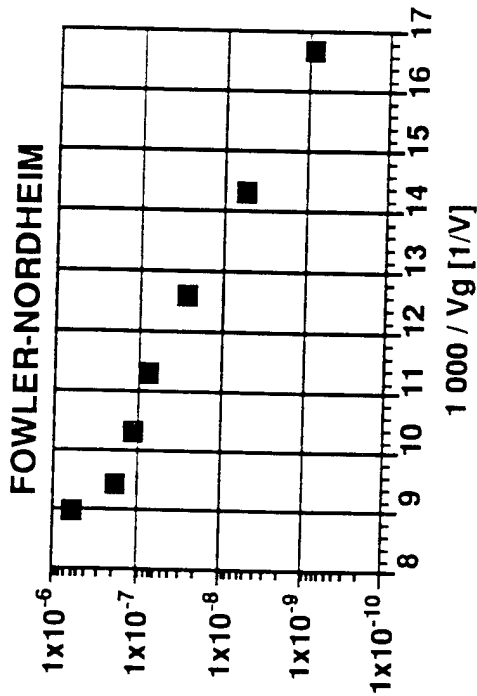
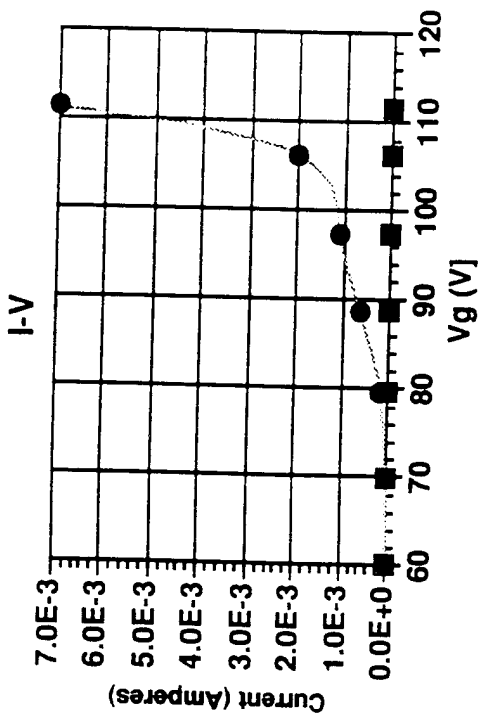


$$I/V_g^2 = 1.218E-2 \cdot \exp(-1499/V_g)$$

$$R^2 = 0.955$$



ELECTRICAL PERFORMANCE - 44, 480 ARRAY



$$I/V_g^2 = 4.93E-4 * \exp(-794/V_g)$$

$$R^2 = 0.985$$



LOW WORK FUNCTION COATINGS

• MOTIVATION

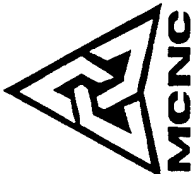
$$\Delta g/g \approx (\phi_{si}/\phi_c)^{3/2} - 1$$

$$V_c/V_{si} \approx (\phi_c/\phi_{si})^{3/2}$$

- *INCREASE TRANSCONDUCTANCE
- *DECREASE GATE VOLTAGE
- *IMPROVE EMISSION STABILITY

• CANDIDATE MATERIALS: CONDUCTIVE, THERMALLY, MECHANICALLY, CHEMICALLY STABLE, COMPATIBLE WITH PROCESS FLOW

• PROCESS OPTIMIZED FOR DEPOSITION OF TaN FILMS (REACTIVE SPUTTERING OF Ta IN NITROGEN ATMOSPHERE)



SUMMARY

- ELECTRICAL PERFORMANCE (DC CONTINUOUS MODE):
 - * EMISSION CURRENTS: UP TO 7 mA FOR GATE VOLTAGE BELOW 200 V
 - * MAXIMUM CURRENT DENSITY: 7 A/cm²
- LARGEST ARRAY TO YIELD: 44, 490 EMITTERS
- PLANS FOR FUTURE DEVICE DEVELOPMENT:
 - * INTEGRATION OF LOW WORK FUNCTION COATINGS INTO THE DEVICE PROCESS SEQUENCE
 - * EVALUATION OF ALTERNATIVE METALLIZATION SCHEMES FOR THE GATE ELECTRODE
 - * PURSUING FURTHER IMPROVEMENT IN DEVICE GEOMETRY AND UNIFORMITY OF CRITICAL PROCESS STEPS